REMARKS

Present Status of the Application

Claims 1-15 are pending of which claims 1-3, 5-7, 10, 12 and 14-15 have been amended to more explicitly describe the claimed invention. It is believed that no new matter is added by way of amendments made to claims or otherwise to the application. For at least the reasons discussed below, Applicants respectfully submit that the updated claims 1-15 patently define over prior art of record and reconsideration of this application is respectfully requested.

Claim Rejections – under 35 U.S.C. 112

Claims 2,6,7,10,11,12,14,15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly point out and claim the subject matter which applicant regards as the invention.

Applicants would like to thank the Examiner for pointing out the informalities in the claims. Accordingly, claims 2, 3, 5-7, 10, 12 and 14-15 are amended to provide proper antecedent basis. Therefore, withdrawal of the rejection is requested.

Claim Rejections - under 35 USC 102(e)

The Office Action rejected Claims 1,5,9 and 13 under 35 U.S.C. 103(e) as being anticipated over U S Patent No. 6,392,496 (Lee et al, hereinafter referred to Lee).

Applicants respectfully disagree and traverse the above rejections based the following reasons.

Nevertheless, Applicants have amended claim 1 to recite "a phase digital converter for comparing a feedback signal with a feedback frequency". Support for the amendment can be found in paragraphs [0015] and [0019] in the specification. The specification discloses "The phase digital converter 204 couples with the output of the pre-divider 202 to output a phase-adjusting value according to the comparable input frequency, a feedback frequency, and a sampling frequency."

Lee discloses "a phase difference computing circuit configured to compare a first clock signal and a second clock signal supplied by the VOC, and the phase difference computing

circuit outputs a phase difference." Lee fails to teach, suggest or disclose "a phase digital converter for comparing a feedback signal with a feedback frequency and a reference signal at a reference frequency, sampling the compared result at a predetermined frequency" as recited in the amended claim 1. In addition. Lee fails to teach , suggest or disclose "a post-divider for feeding back and dividing down the output signal to the phase digital converter based upon a predetermined post adjusting value" as recited in the amended claim 1. Therefore, claim 1 as well as its dependent claims 5, 9 and 13 are not anticipated by Lee.

Claims 1,5,6,9,11,13 are rejected under 35 U.S.C. 103(e) as being anticipated by U S Patent No. 5,856,762 (Wereker et al, hereinafter referred to Wereker).

Applicants respectfully disagree and traverse the above rejections based the following reasons. Wereker discloses a phase-lock loop that utilizes a course control device as a digital phase-locked loop, in which the damping frequency and natural frequency of the phase-locked loop is independent of functions in technology parameters. However, like Lee, Wereker fails to teach , suggest or disclose "a phase digital converter for comparing a feedback signal with a feedback frequency and a reference signal at a reference frequency, sampling the compared result at a predetermined frequency" as recited in the amended claim 1.In addition. Wereker fails to teach, suggest or disclose "a post-divider for feeding back and dividing down the output signal to the phase digital converter based upon a predetermined post adjusting value" as recited in the amended claim 1. Therefore, claim 1 as well as its dependent claims 5, 6, 9, 11, 13 are not anticipated by Wereker.

Claims 1, 5, 6, 9, 11, 13 *are rejected under 35 U.S.C. 103(e) as being anticipated by Walter T. Bax(IEEE Journal of solid state circuit vol. 36, hereinaftyer Walter T. Bax).*

Applicants respectfully disagree and traverse the above rejections based the following reasons. Walter T. Bax only discloses a phase-locked loop that uses a VOC, a phase difference detector for comparing a feedback signal and a reference signal. Walter T.Bax fails to teach, suggest or disclose "a phase digital converter for comparing a feedback signal with a feedback

frequency and a reference signal at a reference frequency, sampling the compared result at a predetermined frequency" as recited in the amended claim 1. Therefore, claim 1 as well as its dependent claims 5, 6 9, 11 and 13 are not anticipated by Walter T.Bax.

Claims 2, 4, 6, 8, 11 , 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Berry (U.S. 6,366,174, hereinafter referred to "Berry")

Claims 2, 4, 12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wereker in view of Berry

Claims 2, 4, 12, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bax in view of Berry

Applicants respectfully disagree and traverse the above rejections based the following reasons. Berry cannot cure the deficiencies of Lee, Wereker, and Bax as discussed above. Therefore, claim 1 as well as its dependent claims are patentable over Lee, Wereker, Bax, and Berry.

Furthermore, these dependent claims contain features that further distinguish over the cited prior art. Berry discloses a method and apparatus for providing a clock generation circuit for digitally controlled frequency or spread spectrum clocking. However, Berry fails to teach, suggest or disclose the preceding phase digital converter 204 and the digital-to-analog voltage converter 205. That is, Berry does not disclose "converting analog signal to digital signal (i.e. phase adjusting value) by the phase digital converter 204, and then converting the digital phase adjusting value to analog adjusting value" as recited in the amended claims 6, 12 and 14.

For the above reasons, claims 1, 2, 4, 8, 11, 13 and 15 are patentable over Lee, Wereker, Bax, and Berry.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-15 of the present application patently define over the prior art and are in proper condition for allowance.

Application No.: 10/058,681 **Docket No.: JCLA7301**

If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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